Patent No. 5,767,549, hereinafter Chen).

Applicants acknowledge with gratitude the indication that Claims 6-16 and 19 would be allowed if rewritten as indicated.

Before turning to the outstanding rejection for obviousness, it is believed that a brief review of the present invention would again be helpful. In this respect, the present invention is directed to a method of designing a semiconductor device having an SOI structure in which the operating speed is not effected so as to become unstable at frequencies greater than 500 MHZ. To accomplish this, the design criteria used is the forming of such an SOI structure which satisfies the equation $R \cdot C \cdot f < 1$ where f, R, and C are specifically defined in both the claims and specification.

In another aspect of the invention, an MOS transistor having an SOI structure is formed using a designing method in which a layout pattern of the MOS transistor is determined to satisfy the expression $(R \cdot C)/td < 1$ where $td \leq 50$ ps, with the parameters td, R, and C again having specific claim and disclosure definitions.

In addition to the method of making such devices, the devices made by these methods are also claimed.

Turning to the outstanding rejection of Claim 1 under 35 U.S.C. §103 as unpatentable over Iwamatsu in view of Agari and Chen, it is first noted that the Action in effect acknowledges that Iwamatsu does not teach the "determining a layout pattern" specified in Claim 1 as a layout pattern of an MOS transistor formed on an SOI layer that will "satisfy the conditional expression $R \cdot C \cdot f < 1$ where C = the gate capacitance of said MOS transistor, R = the resistance of a fixed potential transmission path extending from said at least one body contact to said body region, and f = the operating frequency of said predetermined clock, and

$f \geq 500$ MHZ." To whatever extent the device of Iwamatsu has a body region and a fixed potential transmission path extending between it to a body contact, there is no way to know the resistance of this transmission path, the gate capacitance of the MOS transistor, much less that the claimed value of R (the resistance of the fixed potential transmission path extending from the body contact to the body region) · C(the gate capacitance of the MOS transistor over the body region on a gate oxide film) · f (apparently 2.5 GHz) is less than 1. In order to suggest that the artisan would have made $R \cdot C \cdot f$ ($f \geq$ 500MHz) less than 1, the Action relies upon the teachings of Agari and Chen.

In this respect, the Action first looks to Agari and asserts that it teaches designing a semiconductor device in a manner "minimizing RC delay from the resistance value and the capacitance value at each wiring part" (see the bottom of page 2 of the Action). Chen is then said to teach doping "the body of an SOI MOS transistor [to] minimize the RC time constant due to the body link." Even if these teachings of Agari and Chen are used to modify the apparent method used to make the device of Iwamatsu, they at best teach including a step of determining an optimum wiring line width and spacing to result in minimizing RC delay as to the wiring lines shown in the upper portion of Fig. 1 of Iwamatsu as taught by Agari and a separate doping step to dope body links between body contacts and MOS transistors so that these body links themselves have a body link RC time constant as short as or less than 1 nsec.

The Action appears to suggest (at the top of page 3) that Agari somehow teaches minimizes the RC time constant of a body contact because of the improperly extracted reference to a "wiring part" at the bottom of page 2 of the Action. However, it is clear that Agari actually teaches the optimizing of wiring line widths and spacings in terms of minimizing the RC delay of a "wiring part," where the term "wiring" is one the artisan would

not use to describe a body contact portion. Thus, when the "PURPOSE" and all of the "CONSTITUTION" portions of the "ABSTRACT" are read together to understand what Agari is referring to as a "wiring part" and the typical use of the term "wiring" is considered, it is clear that line width and spacing are relative to standard surface wiring and this width and spacing of the "wiring part" are controlled to minimize RC delay by controlling values of resistance and capacitance corresponding thereto. In this last regard, it is well established to be "impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art" (In re Wesslau, 147 USPQ 391, 393 (CCPA 1965)).

Moreover, even if Agari is assumed to somehow teach minimizing the RC time constant of a body contact, the body contact of Chen is just that, not any of the doped body links disclosed to be between body contacts and MOS transistors also taught by Chen. While Chen further refers to the RC time constant of a region 20 in Fig. 1, this RC time constant is not at all concerned with region 32 illustrated in Fig. 1 of Chen.

In the final analysis, what Claim 1 requires is the use of a layout pattern of an MOS transistor formed on an SOI layer that will "satisfy the conditional expression $R \cdot C \cdot f > 1$ where C = the gate capacitance of said MOS transistor, R = the resistance of a fixed potential transmission path extending from said at least one body contact to said body region, and f = the operating frequency of said predetermined clock, and $f \geq 500$ MHZ" (emphasis added). None of Iwamatsu, Agari, or Chen teach any reason at all to consider multiplying the resistance value R of a fixed potential transmission path extending from a body contact to a body region of the nature claimed by the capacitance value C of a gate of an MOS transistor

formed on an oxide film over the body region and multiplying the result by a clock frequency f that is equal to or greater than 500 MHZ and insuring that the final result is greater than one.

In addition to lacking any evidence that the artisan would have some reason to consider the product of the resistance value R of a fixed potential transmission path extending from a body contact to a body region of the nature claimed and the capacitance value C of a gate of an MOS transistor formed on an oxide film over the body region to be important to control, the Action further lacks any evidence that the artisan would have a prior art based reason to believe that this RC product having an R value and a C value from different elements is somehow a measure of how quickly the signal decays as stated at the top of page 3 of the Action. Similarly lacking is some prior art based reason to believe that this particular RC product having an R value determined by an interior body region and a C value related to a gate electrode over an oxide layer of transistor should be minimized as to a clock signal period so as to produce some desired beneficial result. As noted by In re Sporck, 133 USPQ 360, 364 (CCPA 1962):

> Obviousness is a legal conclusion which we are required to draw from facts appearing in the record or of which judicial notice may be taken. Thus before we can conclude that any disclosed invention is 'obvious' under the conditions specified in 35 U.S.C. 103, we must evaluate facts from which to determine (1) what was shown in the prior art at the time the invention was made, and (2) the knowledge which a person of ordinary skill in the art possessed at the time the invention was made. Here, neither the record nor the facts of which we are able to take judicial notice supplies the factual data necessary to support the legal conclusion of obviousness of the invention at the time it was made. We are unwilling to substitute speculation and hindsight appraisal of the prior art for such factual data.

Turning to Claim 2, it is noted that this claim is similar to Claim 1 as to the method of

designing that is recited and the semiconductor device to be designed. The differences relate to the requirements of Claim 2 that relate to a signal propagation delay time being provided instead of the Claim 1 operating frequency and the determining of the layout pattern being based on this signal propagation delay time instead of the Claim 1 operating frequency. In this regard, Claim 2 requires the layout pattern to be determined so that $(R \cdot C) / td < 1$ with the definitions of R and C being the same for Claim 2 as for Claim 1 and "td" being the signal propagation delay time of the MOS transistor which must be less than or equal to 50 ps.

Once again relative to Claim 2, it is believed to be clear that if the artisan where to reasonably use the teachings of Agari and Chen to design the device of Iwamatsu, he would merely add a step as to determining an optimum wiring line width and spacing to result in minimizing RC delay as to the wiring lines shown in the upper portion of Fig. 1 of Iwamatsu as taught by Agari and a separate doping step to dope body links between body contacts and MOS transistors so that these body links themselves have a body link RC time constant as short as or less than 1 nsec. This is not the method set forth by Claim 2.

Similarly, with respect to independent Claim 2, the teachings of Agari cannot be based upon extracting terms out of context and assigning meanings thereto that are not consistent with the meanings clearly used by Agari. See again the Wesslau decision discussed above. The rejection of Claim 2 is also traversed as relying upon an improper interpretation of the language "wiring part" used by Agari just as the rejection of Claim 1 was.

Moreover, and as noted above, even if Agari is assumed to somehow teach minimizing the RC time constant of a body contact, the body contact of Chen is just that, not any of the doped body links disclosed to be between body contacts and MOS transistors also

taught by Chen. What Claim 2 requires, on the other hand, is the use of a layout pattern to form an MOS transistor on an SOI layer that will satisfy the conditional expression (R·C) / td > 1 where C = the gate capacitance of said MOS transistor, R = the resistance of a fixed potential transmission path extending from said at least one body contact to said body region, and td = signal propagation delay time required for the MOS transistor, with td being less than or equal to 50 ps. None of Iwamatsu, Agari, or Chen teach any reason at all to consider multiplying the resistance value R of a fixed potential transmission path extending from a body contact to a body region of the nature claimed by the capacitance value C of a gate of an MOS transistor formed on an oxide film over the body region and multiplying the result by a signal propagation delay time td required for the MOS transistor, with td being less than or equal to 50 ps and insuring that the final result is less than one.

Clearly, the resistance "R" of concern in Claim 2 is again that of a "fixed potential transmission path" extending from a body contact to a body region as discussed above and not the resistance of the wiring line of concern to Agari. In addition none of Iwamatsu, Agari, or Chen teach any reason to use the capacitance "C" of the MOS transistor gate electrode along with this value R of an internal transmission path to form an RC product, much less one that meets the Claim 2 requirement that (R·C) / td <1 with td being less than or equal to 50 ps. Once again, valid rejections can only be made if they are based upon established facts as to the prior art. The rejection of Claim 2 is also traversed because speculation and hindsight based upon applicants' disclosure have again been used as a substitute for facts not of record.

Substantially the same arguments made above as to Claims 1 and 2 apply equally to Claims 3 and 5 which ultimately depend on Claim 1 and Claims 4 and 18 which ultimately

depend on Claim 2. In addition, each of these dependent claims add further features to the base claims which are neither taught nor disclosed by the applied references considered alone or in any proper combination. Accordingly, the rejections of Claims 3-5 and 18 are traversed for the reasons presented above as to base Claims 1 and 2 as well as because there has been no establishment of any *prima facie* case of obviousness as to these additional features which are also not taught or suggested by the references relied upon.

Since no other issues are believed to be outstanding in the present application, it is believed to be clearly in condition for formal allowance. Consequently, an early and favorable action to that effect is earnestly and respectfully requested.

Respectfully submitted,

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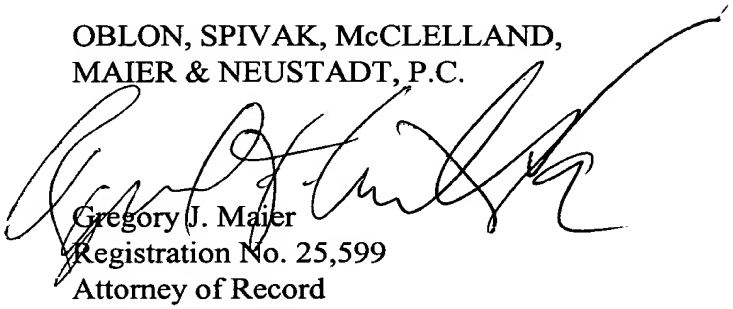

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